74AHC3GU04

Inverter

Rev. 01 — 23 September 2004 Product data sheet

1. General description

The 74AHC3GU04 is a high-speed Si-gate CMOS device. This device provides the inverting single stage function.

2. Features

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- Output capability ±8 mA drive
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C.

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 5 V; C_L = 15 pF		-	2.5	5.5	ns
C_I	input capacitance			-	3.0	10	pF
C_{PD}	power dissipation capacitance		[1] [2]	-	4	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

PHILIPS

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC3GU04DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHC3GU04DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AHC3GU04GM	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 0.95 × 1.95 × 0.5 mm	SOT833-1

5. Marking

Table 3: Marking

Type number	Marking code
74AHC3GU04DP	AU04
74AHC3GU04DC	AU4
74AHC3GU04GM	AU4

6. Functional diagram

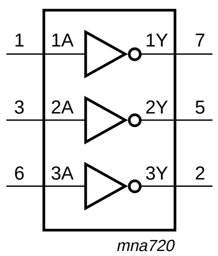


Fig 1. Logic symbol.

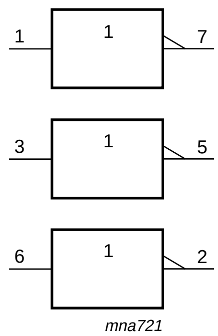


Fig 2. IEC logic symbol.

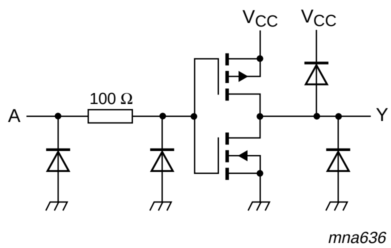


Fig 3. Logic diagram.

7. Pinning information

7.1 Pinning

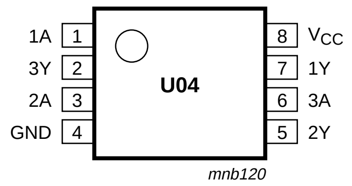


Fig 4. Pin configuration TSSOP8 and VSSOP8.

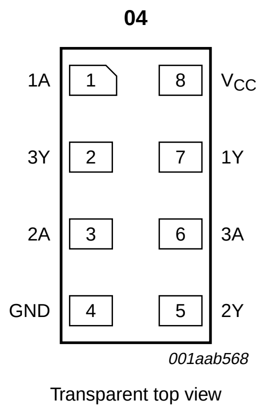


Fig 5. Pin configuration XSON8.

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
1A	1	data input
3Y	2	data output
2A	3	data input
GND	4	ground (0 V)
2Y	5	data output
3A	6	data input
1Y	7	data output
V_{CC}	8	supply voltage

8. Functional description

8.1 Function table

Table 5: Function table [1]

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	supply voltage			–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V		-	–20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output source or sink current	$V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±75	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C		-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

10. Recommended operating conditions

Table 7: Recommended operating operations

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	operating ambient temperature	see Section 11 and Section 12	–40	+25	+125	°C
t_r, t_r	input rise and fall times	V_{CC} = 3.3 V ± 0.3 V	-	-	100	ns/V
		V_{CC} = 5 V ± 0.5 V	-	-	20	ns/V

11. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.7	-	-	V
		V_{CC} = 3.0 V	2.4	-	-	V
		V_{CC} = 5.5 V	4.4	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.3	V
		V_{CC} = 3.0 V	-	-	0.6	V
		V_{CC} = 5.5 V	-	-	1.1	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.0 V; I_O = –50 μA	1.9	2.0	-	V
		V_{CC} = 3.0 V; I_O = –50 μA	2.9	3.0	-	V
		V_{CC} = 4.5 V; I_O = –50 μA	4.4	4.5	-	V
		V_{CC} = 3.0 V; I_O = –4.0 mA	2.58	-	-	V
		V_{CC} = 4.5 V; I_O = –8.0 mA	3.94	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.0 V; I_O = 50 μA	-	0	0.1	V
		V_{CC} = 3.0 V; I_O = 50 μA	-	0	0.1	V
		V_{CC} = 4.5 V; I_O = 50 μA	-	0	0.1	V
		V_{CC} = 3.0 V; I_O = 4.0 mA	-	-	0.36	V
		V_{CC} = 4.5 V; I_O = 8.0 mA	-	-	0.36	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	μA
C_I	input capacitance		-	3.0	10	pF
T_{amb} = –40 °C to 85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.7	-	-	V
		V_{CC} = 3.0 V	2.4	-	-	V
		V_{CC} = 5.5 V	4.4	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.3	V
		V_{CC} = 3.0 V	-	-	0.6	V
		V_{CC} = 5.5 V	-	-	1.1	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –50 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.9	-	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.48	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.8	-	-	V

Table 8: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50\ \mu A$; $V_{CC} = 2.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 3.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 4.5\ V$	-	-	0.1	V
		$I_O = 4.0\ mA$; $V_{CC} = 3.0\ V$	-	-	0.44	V
		$I_O = 8.0\ mA$; $V_{CC} = 4.5\ V$	-	-	0.44	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 5.5\ V$	-	-	10	µA
C_I	input capacitance		-	-	10	pF
$T_{amb} = -40\ °C$ to $+125\ °C$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\ V$	1.7	-	-	V
		$V_{CC} = 3.0\ V$	2.4	-	-	V
		$V_{CC} = 5.5\ V$	4.4	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\ V$	-	-	0.3	V
		$V_{CC} = 3.0\ V$	-	-	0.6	V
		$V_{CC} = 5.5\ V$	-	-	1.1	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50\ \mu A$; $V_{CC} = 2.0\ V$	1.9	-	-	V
		$I_O = -50\ \mu A$; $V_{CC} = 3.0\ V$	2.9	-	-	V
		$I_O = -50\ \mu A$; $V_{CC} = 4.5\ V$	4.4	-	-	V
		$I_O = -4.0\ mA$; $V_{CC} = 3.0\ V$	2.40	-	-	V
		$I_O = -8.0\ mA$; $V_{CC} = 4.5\ V$	3.70	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50\ \mu A$; $V_{CC} = 2.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 3.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 4.5\ V$	-	-	0.1	V
		$I_O = 4.0\ mA$; $V_{CC} = 3.0\ V$	-	-	0.55	V
		$I_O = 8.0\ mA$; $V_{CC} = 4.5\ V$	-	-	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	2.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 5.5\ V$	-	-	40	µA
C_I	input capacitance		-	-	10	pF

12. Dynamic characteristics

Table 9: Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $t_r = t_f \leq 3.0$ ns. See Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}, t_{PLH}	propagation delay nA to nY	see Figure 6					
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[1]	-	3.0	7.1	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	[1]	-	4.3	10.6	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[2]	-	2.5	5.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[2]	-	3.5	7.0	ns
C_{PD}	power dissipation capacitance		[3] [4]	-	4	-	pF
T_{amb} = −40 °C to 85 °C							
t_{PHL}, t_{PLH}	propagation delay nA to nY	see Figure 6					
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		1.0	-	8.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF		1.0	-	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		1.0	-	6.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF		1.0	-	8.0	ns
T_{amb} = −40 °C to 125 °C							
t_{PHL}, t_{PLH}	propagation delay nA to nY	see Figure 6					
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		1.0	-	10.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF		1.0	-	13.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		1.0	-	7.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF		1.0	-	9.0	ns

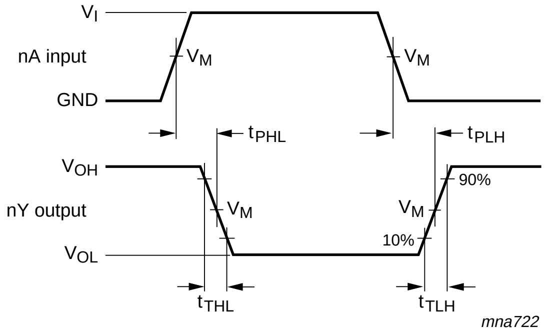
[1] Typical values are measured at V_{CC} = 3.3 V.

[2] Typical values are measured at V_{CC} = 5.0 V.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

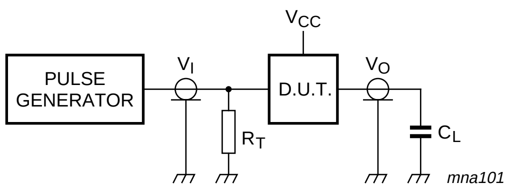
[4] The condition is V_I = GND to V_{CC}.

13. AC waveforms



V_M = 50 %; V_I = GND to V_{CC}.

Fig 6. Input (nA) to output (nY) propagation delays.



Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance. (See Section 12 for values).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 7. Load circuitry for switching times.

13.1 Typical transfer characteristics

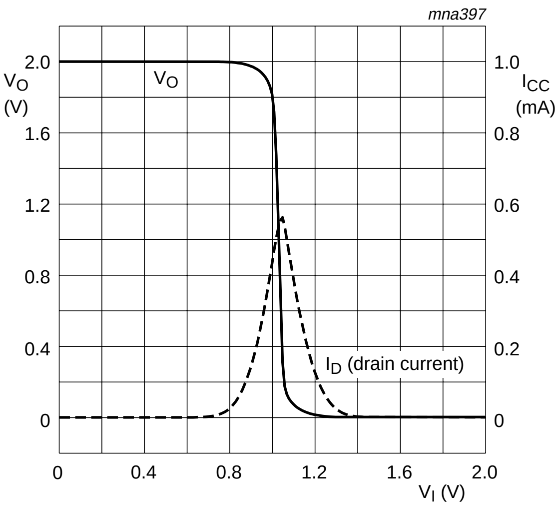


Fig 8. V_{CC} = 2.0 V; I_O = 0 A.

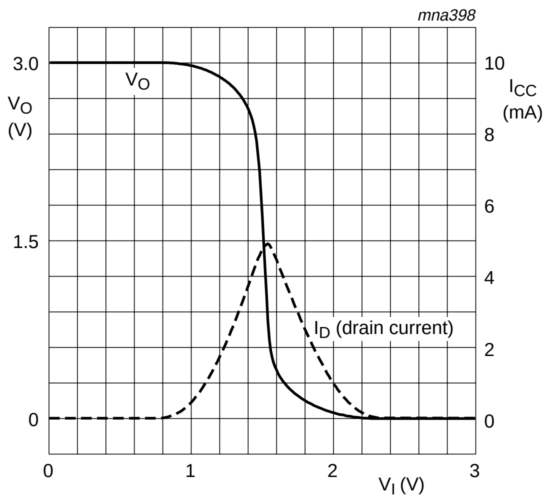


Fig 9. V_{CC} = 3.0 V; I_O = 0 A.

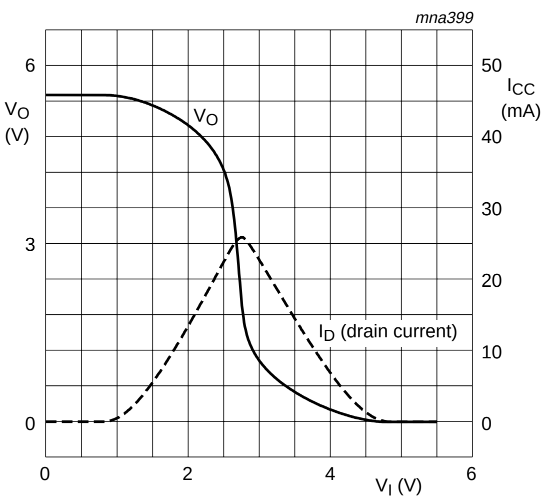
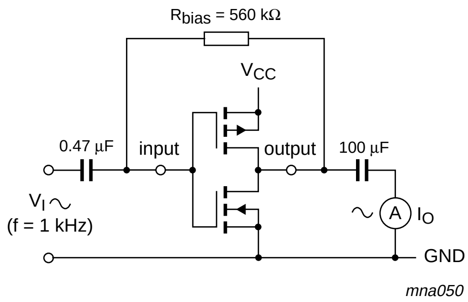


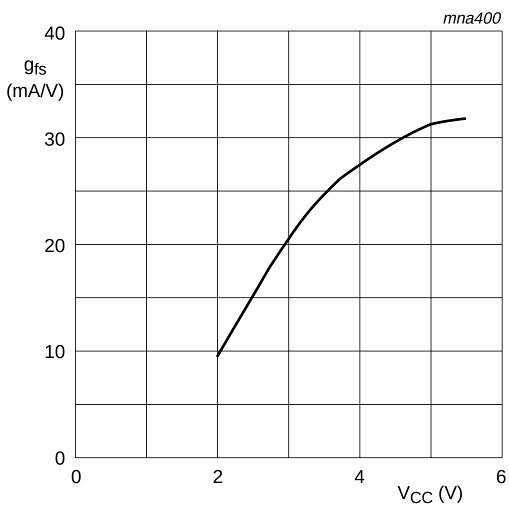
Fig 10. V_{CC} = 5.5 V; I_O = 0 A.

13.2 Forward transconductance



$g_{fs} = \Delta I_O / \Delta V_I$; V_O is constant.

Fig 11. Test set-up for measuring forward transconductance.



At T_{amb} = 25 °C.

Fig 12. Typical forward transconductance as a function of the supply voltage.

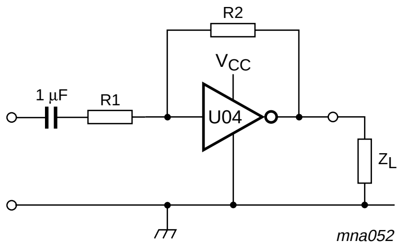
14. Application information

Some applications are:

- Linear amplifier see Figure 13
- In crystal oscillator design see Figure 14.

Remark: All values given are typical unless otherwise specified.

14.1 Linear amplifier



$V_{O(max)(p\text{-}p)} = V_{CC} - 1.5$ V centered at $0.5 \times V_{CC}$.

$$A_u = \frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})}$$

A_{OL} = open loop amplification.

A_u = voltage amplification.

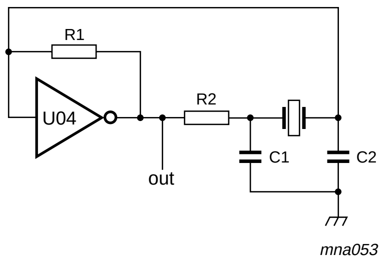
R1 ≥ 3 kΩ; R2 ≤ 1 MΩ.

Z_L > 10 kΩ; A_{OL} = 20 (typical).

Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier.

14.2 Crystal oscillator



C1 = 47 pF (typical).

C2 = 22 pF (typical).

R1 = 1 MΩ to 10 MΩ (typical).

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3 V and f = 1 MHz).

Fig 14. Crystal oscillator configuration.

Table 10: External components for resonator (f < 1 MHz)

Frequency (kHz)	R1 (MΩ)	R2 (kΩ)	C1 (pF)	C2 (pF)
10 to 15.9	22	220	56	20
16 to 24.9	22	220	56	10
25 to 54.9	22	100	56	10
55 to 129.9	22	100	47	5
130 to 199.9	22	47	47	5
200 to 349.9	22	47	47	5
350 to 600	22	47	47	5

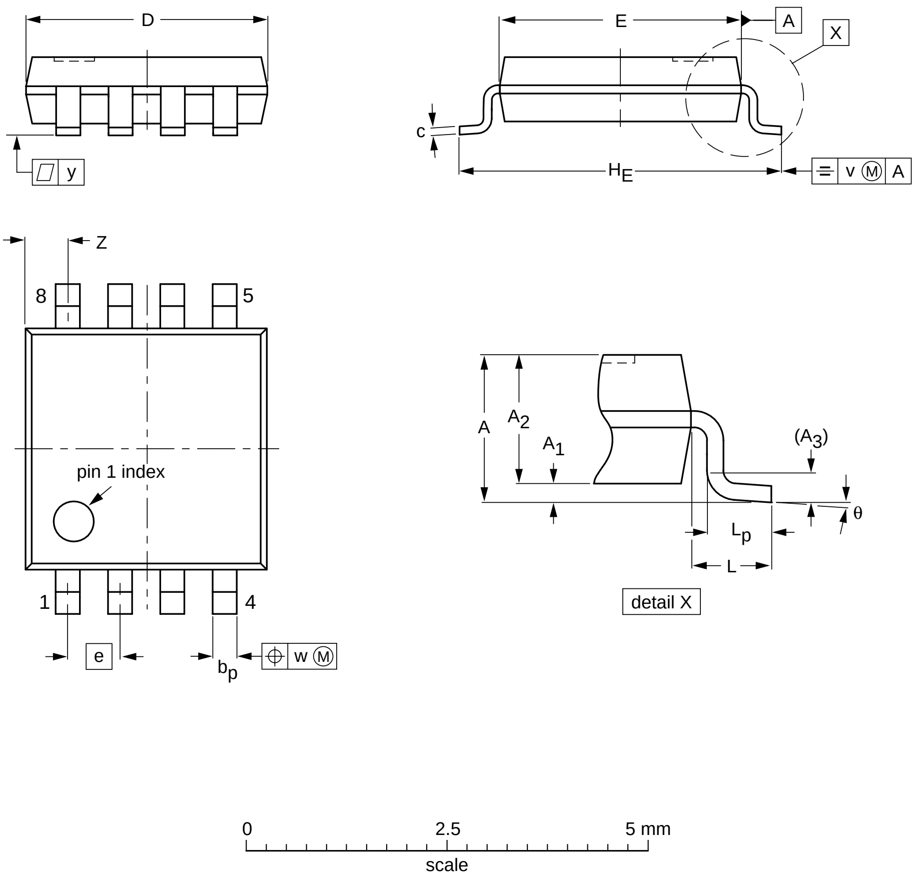
Remark: All values given are typical and must be used as initial set-up.

Table 11: Optimum value for R2

Frequency (kHz)	R2 (kΩ)	Optimum for
3	2.0	minimum required I_{CC}
	8.0	minimum influence due to change in V_{CC}
6	1.0	minimum required I_{CC}
	4.7	minimum influence due to change in V_{CC}
10	0.5	minimum required I_{CC}
	2.0	minimum influence due to change in V_{CC}
14	0.5	minimum required I_{CC}
	1.0	minimum influence due to change in V_{CC}
>14	-	replace R2 by C3 with a typical value of 35 pF

15. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm **SOT505-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

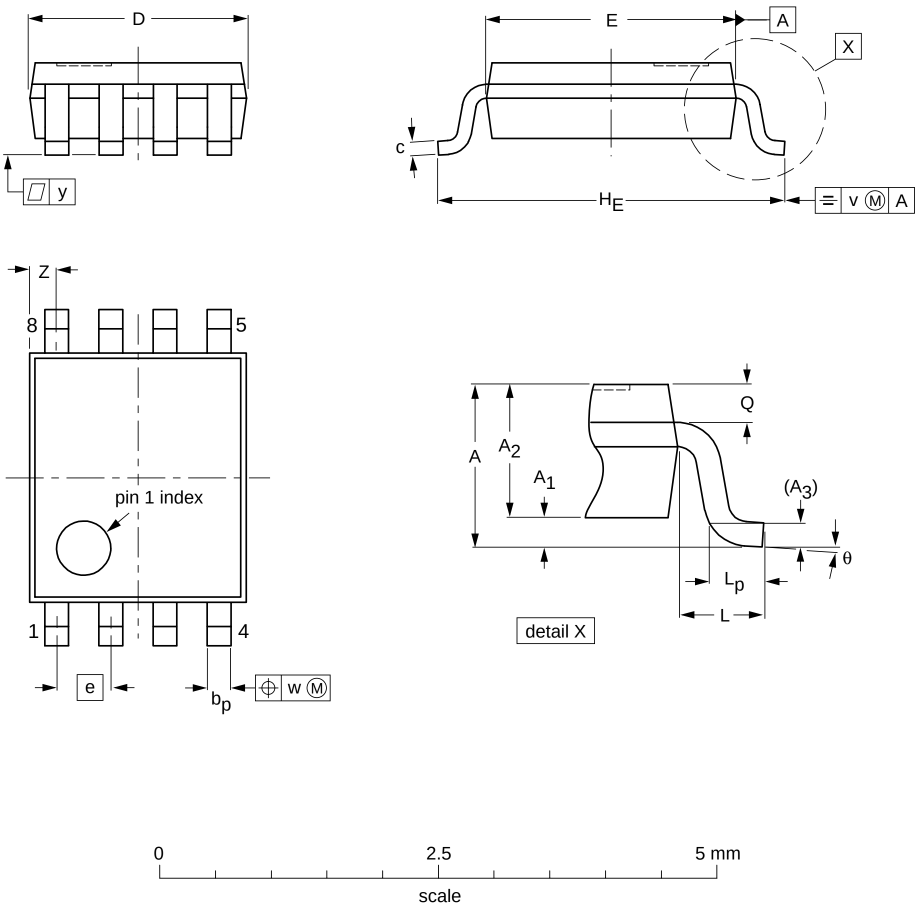
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 15. Package outline SOT505-2 (TSSOP8).

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

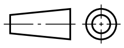
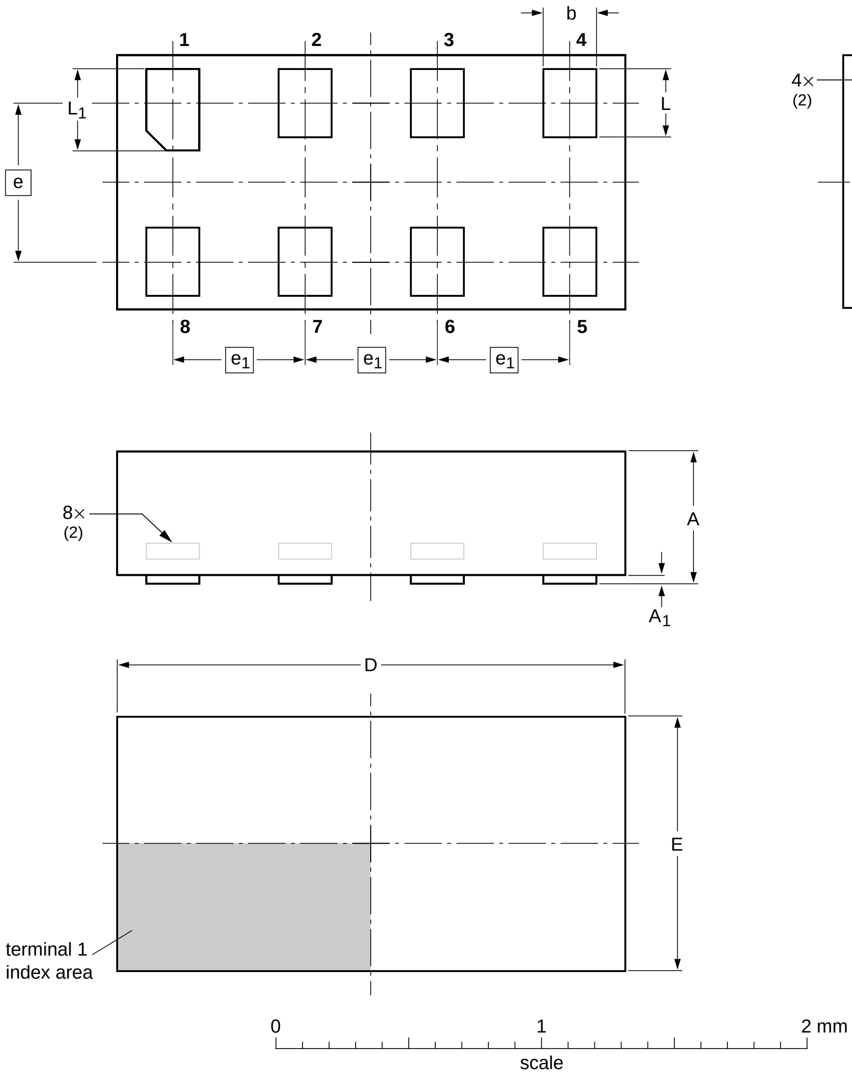
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 16. Package outline SOT765-1 (VSSOP8).

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 0.95 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.0 0.9	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~04-07-15~~ 04-07-22

Fig 17. Package outline SOT833-1 (XSON8).

16. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74AHC3GU04_2	20040923	product data sheet	-	9397 750 13742	74AHC3GU04_1
Modifications:	Addition of SOT833 and changes in Ordering information and ESD protection.				
74AHC3GU04_1	20040305	product data sheet	-	9397 750 12754	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

21. Contents

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